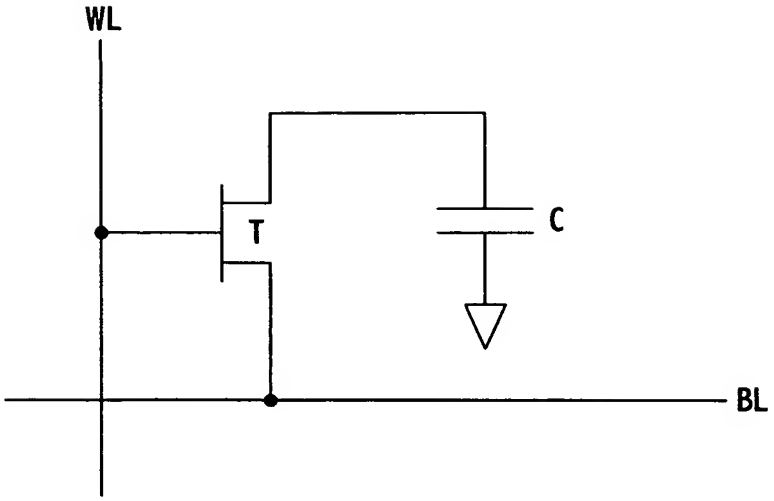
WL
T
C
BL

FIG. 1

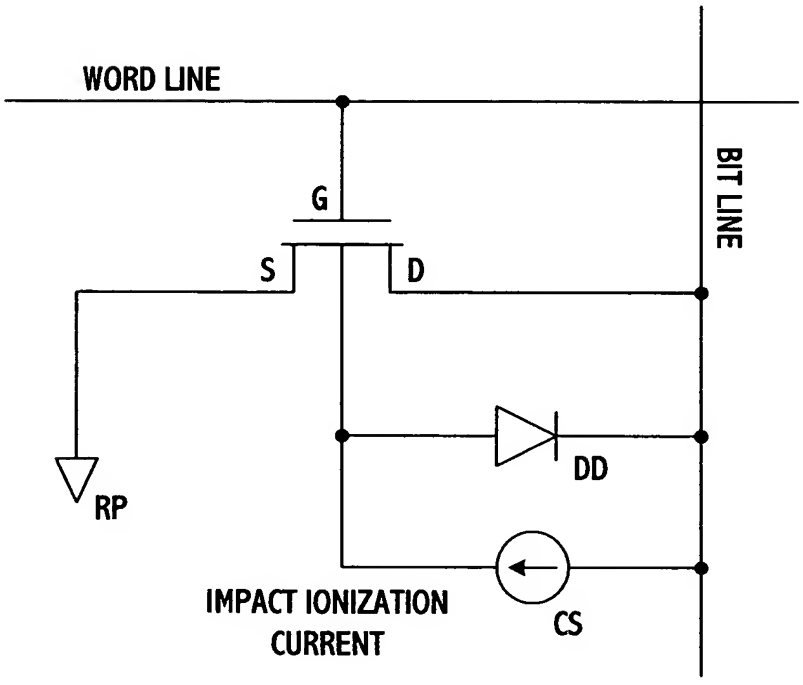
WORD LINE
BIT LINE
G
S
D
DD
RP
IMPACT IONIZATION
CURRENT
CS

FIG. 2

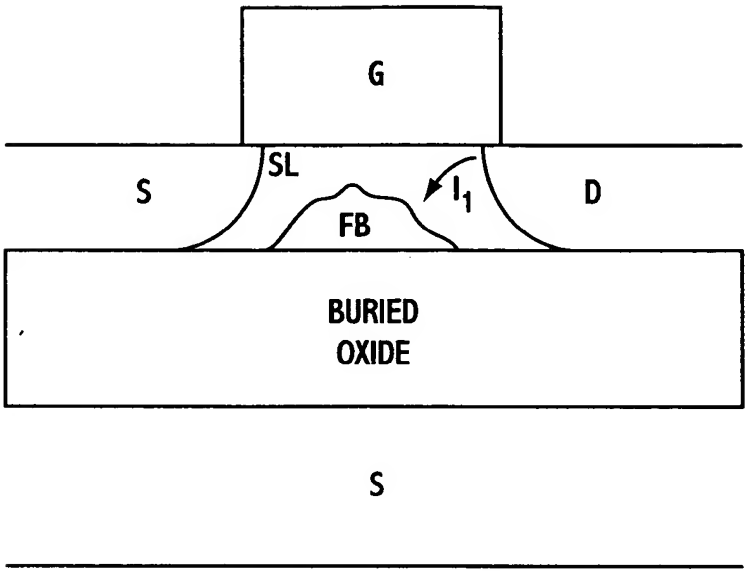

FIG. 3

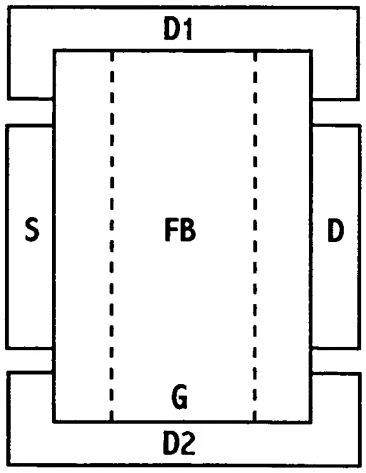

FIG. 4

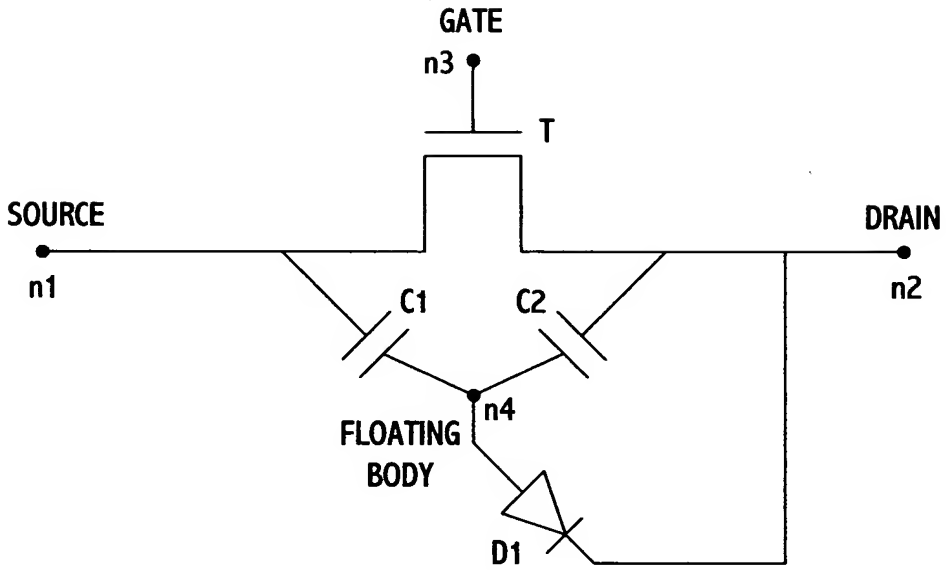

FIG. 5

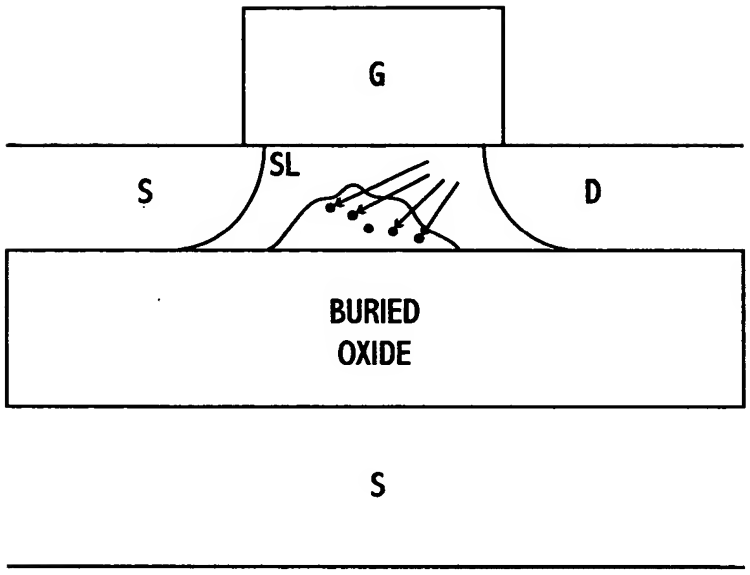

FIG. 6A

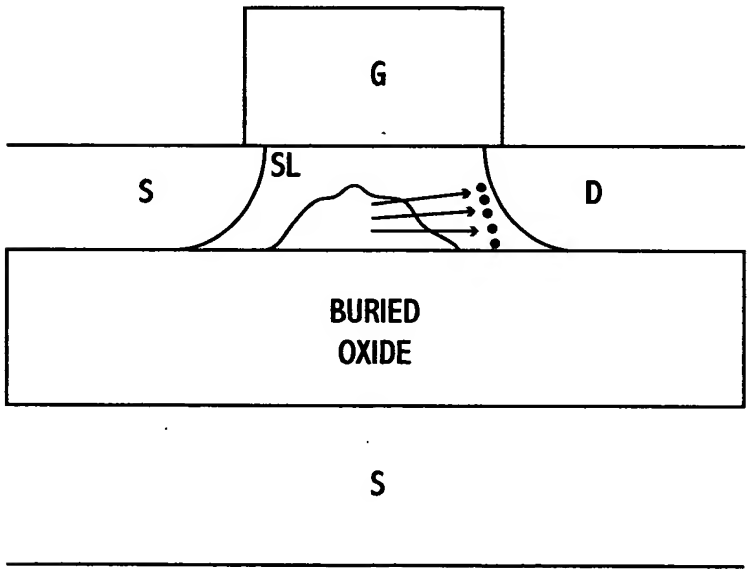

FIG. 6B

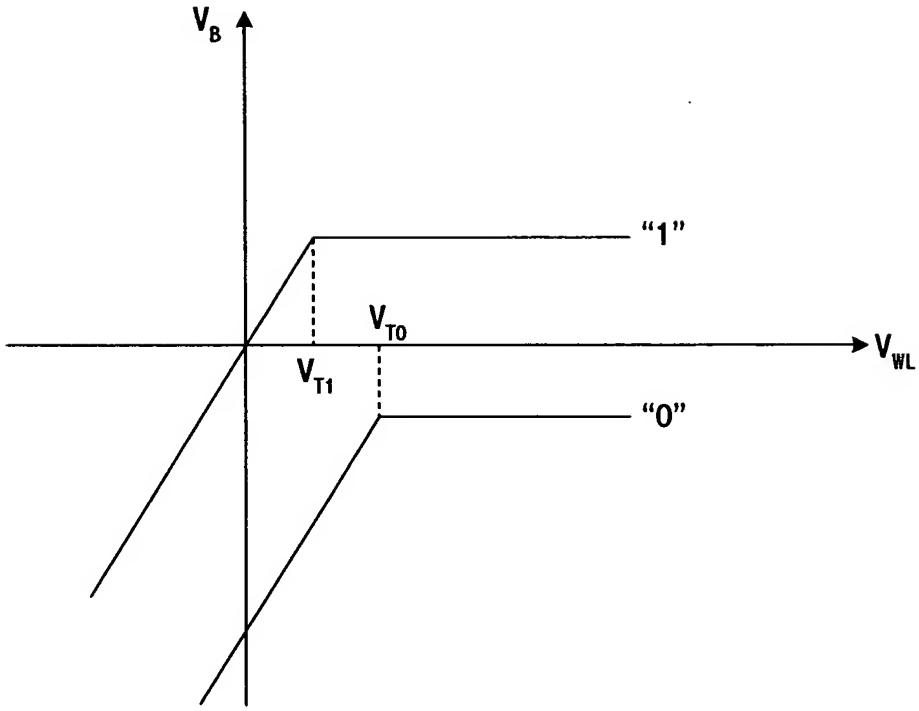

FIG. 7

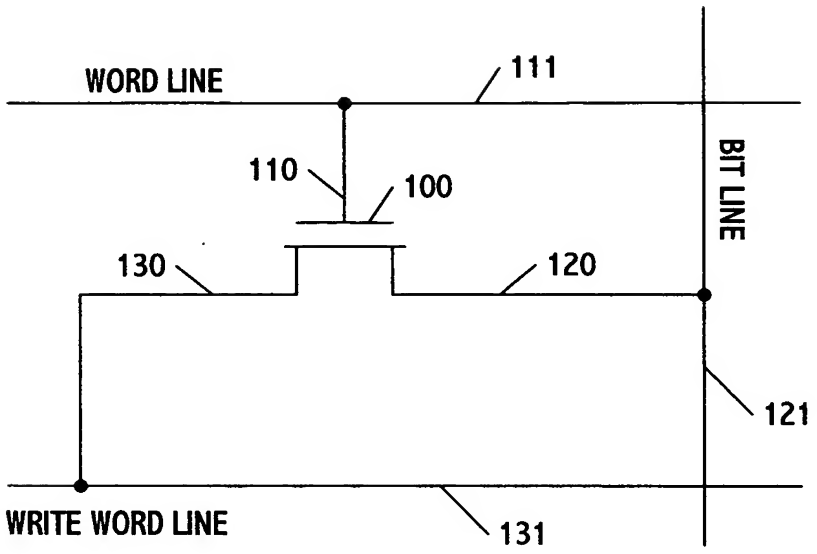
WORD LINE
111
110
100
BIT LINE
130
120
121
WRITE WORD LINE
131

FIG. 8

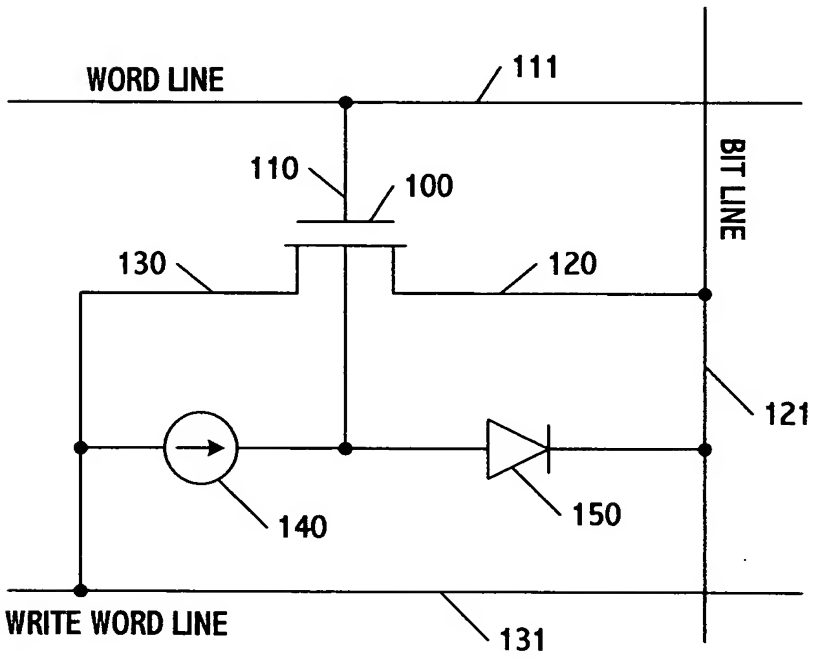
WORD LINE
111
110
100
BIT LINE
130
120
121
140
150
WRITE WORD LINE
131

FIG. 9

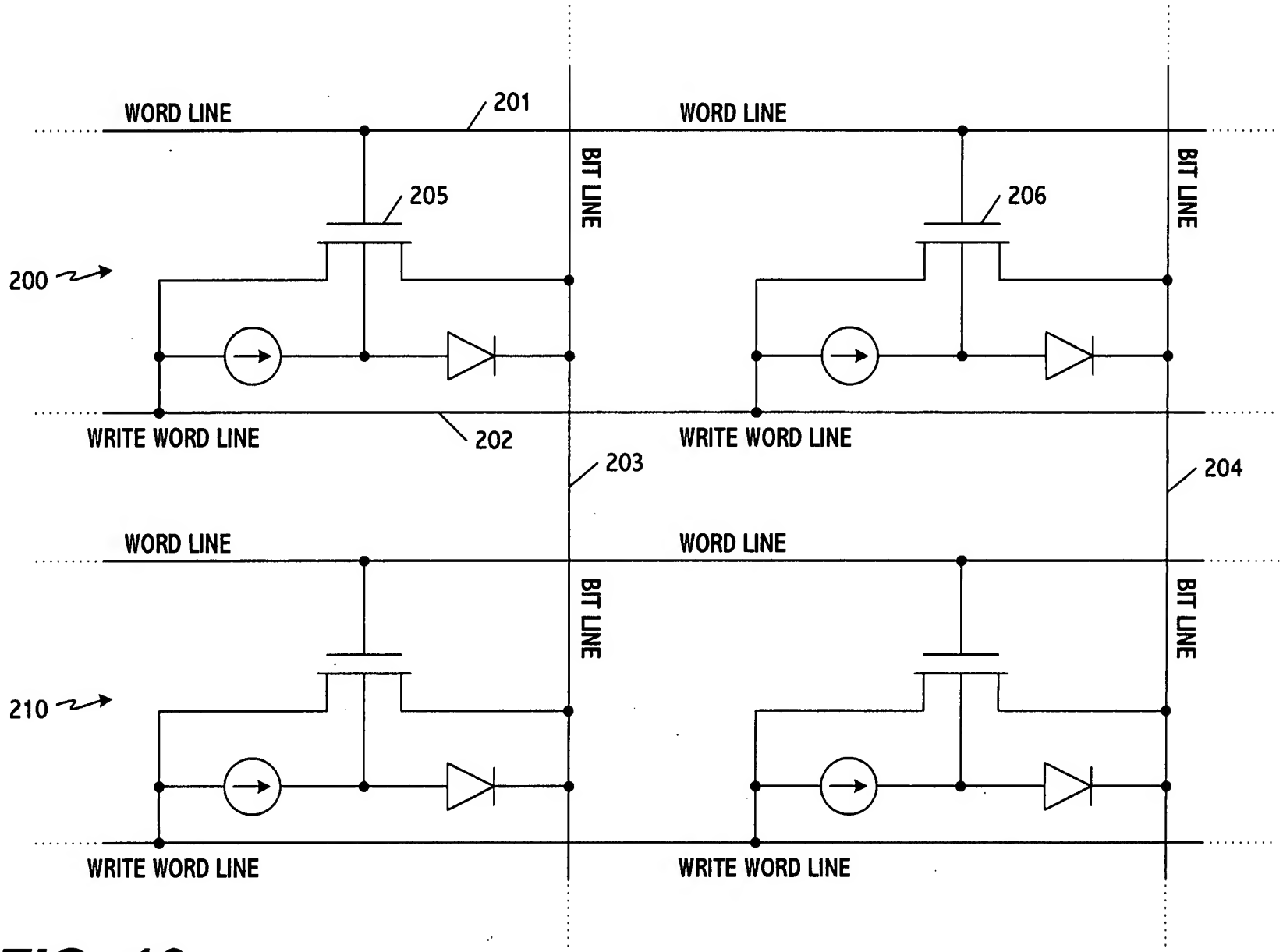
WORD LINE
201
WORD LINE
BIT LINE
205
206
BIT LINE
200
WRITE WORD LINE
202
WRITE WORD LINE
203
204
WORD LINE
WORD LINE
BIT LINE
BIT LINE
210
WRITE WORD LINE
WRITE WORD LINE

FIG. 10

	DRAIN (WRITE WORD LINE)	GATE (WORD LINE)	SOURCE (BIT LINE)
HOLD	LOW	VERY LOW (ACCUMULATED)	LOW
ROW WRITE 1 (IMP. ION. ON)	HIGH	HIGH	LOW
KEEP1/WRITE0 (DIODE OFF/ON)	LOW	MEDIUM TO LOW	LOW/VERY LOW

FIG. 11

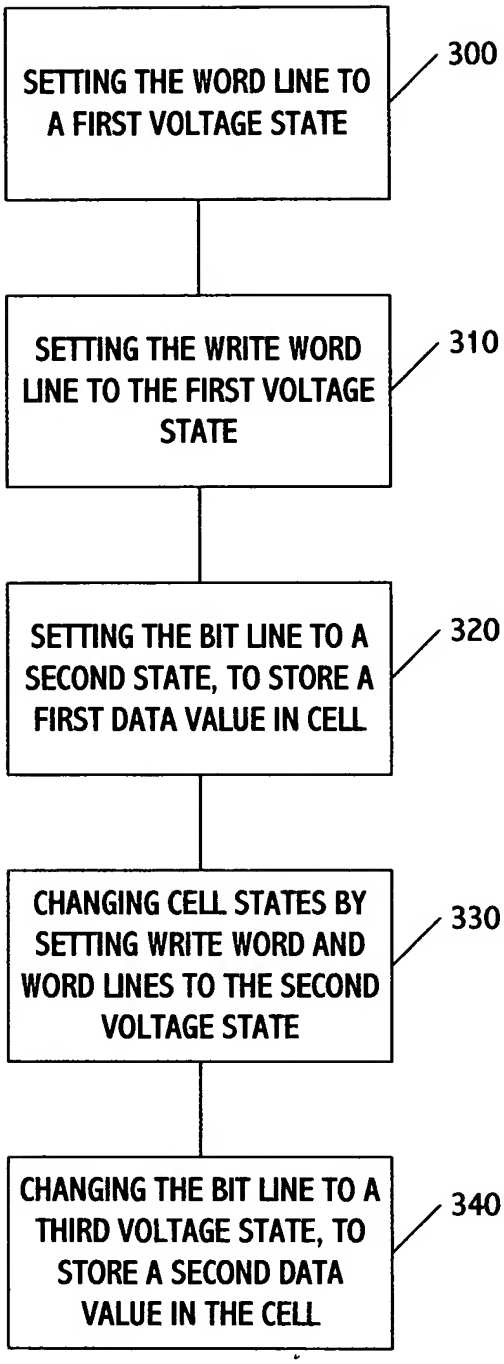
SETTING THE WORD LINE TO A FIRST VOLTAGE STATE
300
SETTING THE WRITE WORD LINE TO THE FIRST VOLTAGE STATE
310
SETTING THE BIT LINE TO A SECOND STATE, TO STORE A FIRST DATA VALUE IN CELL
320
CHANGING CELL STATES BY SETTING WRITE WORD AND WORD LINES TO THE SECOND VOLTAGE STATE
330
CHANGING THE BIT LINE TO A THIRD VOLTAGE STATE, TO STORE A SECOND DATA VALUE IN THE CELL
340

FIG. 12

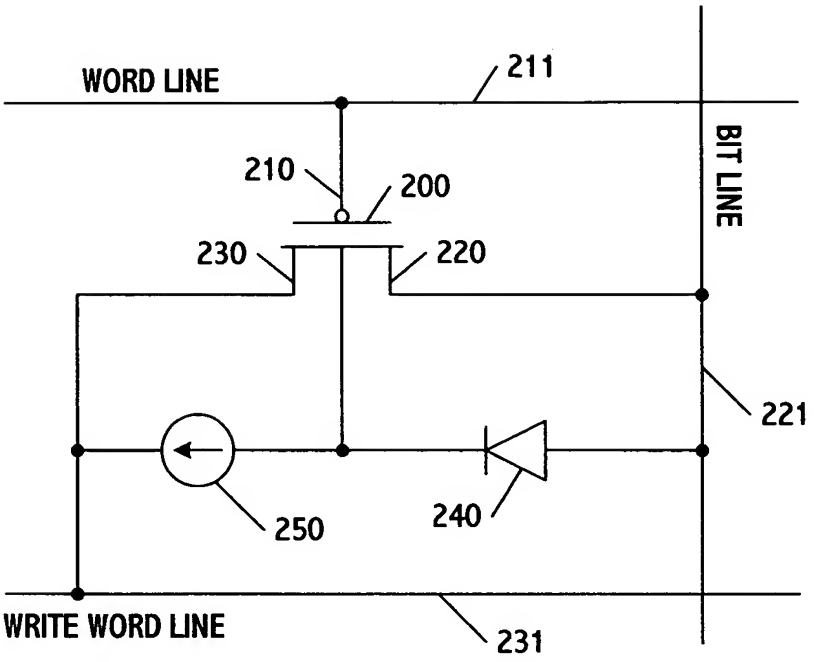

FIG. 13

	DRAIN (WRITE WORD LINE)	GATE (WORD LINE)	SOURCE (BIT LINE)
HOLD	HIGH	VERY HIGH (ACCUMULATED)	HIGH
ROW WRITE 1 (IMP. ION. ON)	LOW	LOW	HIGH
KEEP1/WRITE0 (DIODE OFF/ON)	HIGH	MEDIUM TO HIGH	HIGH/ VERY HIGH

FIG. 14

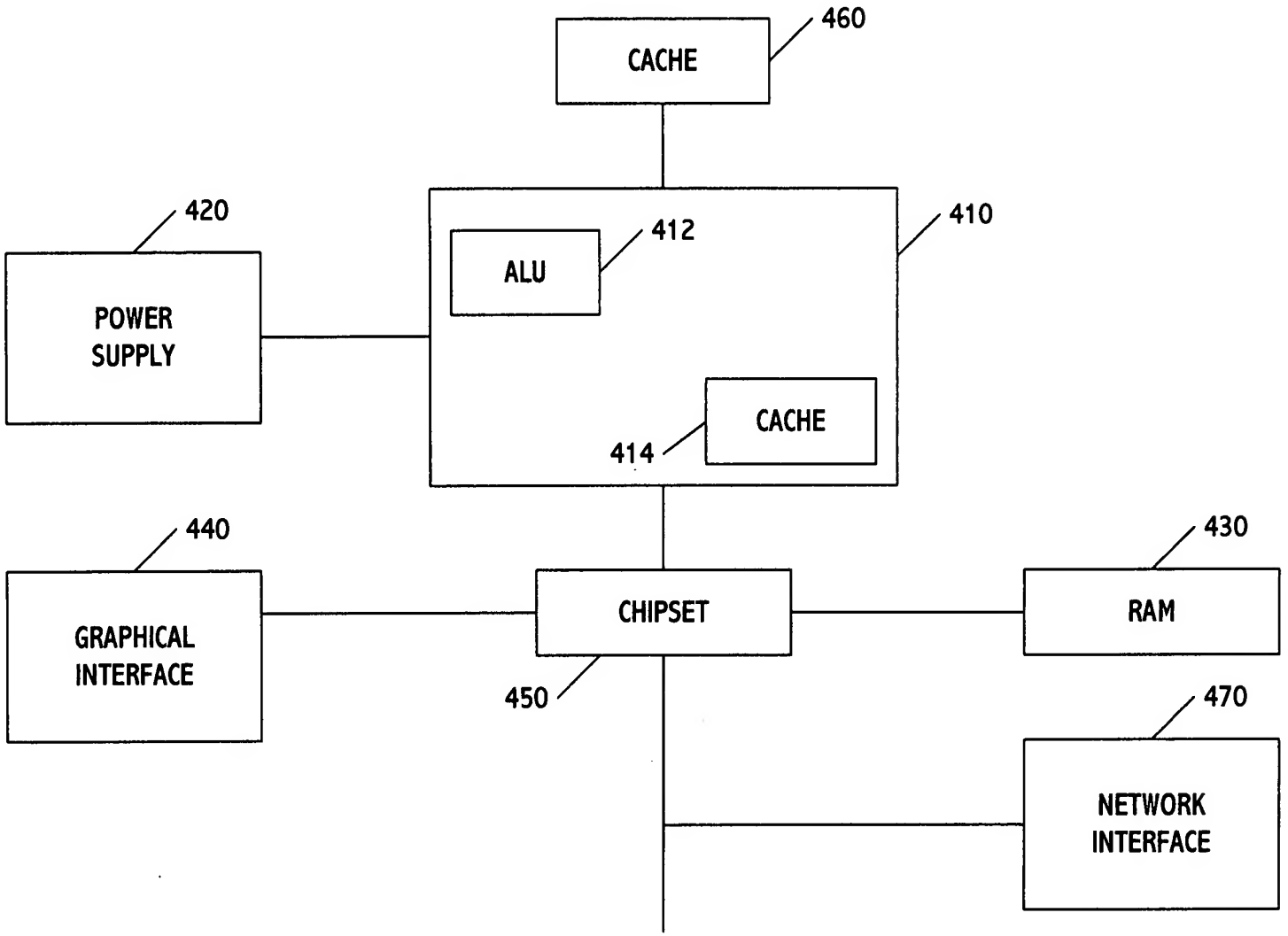
CACHE
460
420
POWER SUPPLY
ALU
412
410
CACHE
414
440
GRAPHICAL INTERFACE
CHIPSET
RAM
430
450
470
NETWORK INTERFACE

FIG. 15